wherein, when the magnitude of said external supply voltage is not larger than that of a predetermined first voltage, the internal supply voltage of said internal power supply means changes at a first rate, when said external supply voltage is between a level exceeding said first voltage and a predetermined second voltage, said internal supply voltage changes at a second rate which is smaller than said first rate, and after said external supply voltage exceeds said second voltage, said internal supply voltage changes at a third rate which is larger than the second rate, wherein said first circuits are fed said internal supply voltage, wherein the magnitude of said internal supply voltage changing at said second rate is <u>not smaller but</u> larger than that of said internal supply voltage changing at said first rate, [and] wherein said internal supply voltage changing at said third rate enables testing of said first circuits<u>, and wherein the magnitude of said internal supply voltage becomes larger without decreasing in proportion to an enlargement of said magnitude of said external supply voltage</u>.

5
~~12.~~ (Twice Amended) A semiconductor integrated circuit [according to claim 11,] comprising:

<u>a chip;</u>

<u>first circuits provided on said chip;</u>

<u>second circuits provided on said chip; and</u>

internal power supply means provided on said chip for reducing an external supply voltage to an internal supply voltage smaller than said external supply voltage within said chip;

wherein, when the magnitude of said external supply voltage is not larger than that of a predetermined first voltage, the internal supply voltage of said internal power supply means changes at a first rate, when said external supply voltage is between a level exceeding said first voltage and a predetermined second voltage, said internal supply voltage changes at a second rate which is smaller than said first rate, and after said external supply voltage exceeds said second voltage, said internal supply voltage changes at a third rate which is larger than the second rate, wherein said first circuits are fed said internal supply voltage, wherein the magnitude of said internal supply voltage changing at said second rate is larger than that of said internal supply voltage changing at said first rate and wherein said internal supply voltage changing at said third rate enables testing of said first circuits;

wherein the change of said internal supply voltage is made inside of said internal power supply means by detecting a change in said external supply voltage;

wherein, when said external supply voltage is between said level exceeding said first voltage and said second voltage, said first circuits are in normal operative

60

states, and wherein, when said external supply voltage exceeds said second voltage, said first circuits are in aging tests>

wherein the third rate of change of said internal supply voltage when said external supply voltage is between a level exceeding said second voltage and a predetermined third voltage is higher than a fourth rate of change of said internal supply voltage after said external supply voltage exceeds said third voltage>

wherein when said external supply voltage is between said first voltage and said second voltage, said internal supply voltage is substantially constant.

Sub. I-2 6

~~13~~. (twice amended) A semiconductor integrated circuit comprising:

a chip;

[loaded] load circuits provided on said chip;

internal power supply means provided on said chip for reducing an external supply voltage to an internal supply voltage smaller than said external supply voltage within said chip and supplying it to said load circuits;

wherein, when the magnitude of said external supply voltage is not larger than that of a predetermined first voltage, the internal supply voltage of said internal power supply means changes at a first rate, when said external supply voltage is between a level exceeding said first voltage and a predetermined second voltage, said

internal supply voltage changes at a second rate which is smaller than said first rate, and after said external supply voltage exceeds said second voltage, said internal supply voltage changes at a third rate which is larger than the second rate, [wherein said load circuits are fed said internal supply voltage,] wherein the magnitude of said internal supply voltage changing at said second rate is <u>not smaller but</u> larger than that of said internal supply voltage changing at said first rate [and] wherein said internal supply voltage changing at said third rate enables testing of said load circuits<u>, and wherein the magnitude of said internal supply voltage becomes larger without decreasing in proportion to an enlargement of said magnitude of said external supply voltage</u>.

Claim 17, line 3, delete "a".

Sub 10
19. (amended) A semiconductor integrated circuit [according to claim 18,] <u>comprising:</u>

<u>a chip</u>

<u>load circuits provide don said chip;</u>

<u>internal power supply means provided on said chip for reducing an external supply voltage to an internal supply voltage smaller than said external supply voltage within said chip and supplying it to said load circuits;</u>

<u>wherein, when the magnitude of said external supply voltage is not larger than that of a predetermined</u>

first voltage, the internal supply voltage of said internal power supply means changes at as first rate, when said external supply voltage is between a level exceeding said first voltage and a predetermined second voltage, said internal supply voltage changes at a second rate which is smaller than said first rate, and after said external supply voltage exceeds said second voltage, said internal supply voltage changes at a third rate which is larger than the second rate, wherein the magnitude of said internal supply voltage changing at said second rate is larger than that of said internal supply voltage changing at said first rate and wherein said internal supply voltage changing at said third rate enables testing of said load circuits;

wherein the change of said internal supply voltage is made inside of said internal power supply means by detecting a change in said external supply voltage;

wherein, when said external supply voltage is between said level exceeding said first voltage and said second voltage, said load circuits are in normal operative states, and wherein, when said external supply voltage exceeds said second voltage said load circuits are in aging tests;

wherein the third rate of change of said internal supply voltage when said external supply voltage is between a level exceeding said second voltage and a predetermined third voltage is higher than a fourth rate of change of said

internal supply voltage after said external supply voltage exceeds said third voltage;

wherein, when said external supply voltage is between said first voltage and said second voltage, said internal supply voltage is substantially constant.

20. (Twice Amended) A semiconductor integrated circuit comprising:

a chip;

a first circuit provided on said chip;

a second circuit provided on said chip;

an internal power supply means, provided on said chip, for supplying an internal supply voltage which is smaller than an external supply voltage;

a reference voltage generating means, provided on said [c hip] chip, for generating a reference voltage;

wherein said reference voltage provided by said reference voltage generating means is fed to said internal power supply means, said internal supply voltage provided by said internal power supply [mean sis] means is fed to said second circuit, and said external supply voltage is fed to said first circuit, [and] wherein, when the magnitude of said external supply voltage is not larger than that of a predetermined first voltage, the internal supply voltage of said internal power supply means changes at a first rate, when said external supply voltage is between a level exceeding said first voltage and a predetermined second voltage, said internal supply voltage changes at a second

rate which is smaller than said first rate, and after said external supply voltage exceeds said second voltage, said internal supply voltage changes at a third rate which is larger than the second rate, wherein the magnitude of said internal supply voltage changing at said second rate is not smaller but larger than that of said internal supply voltage changing at said first rate, [and] wherein said internal supply voltage changing at said third rate enables testing of said second circuit, and wherein the magnitude of said internal supply voltage becomes larger without decreasing in proportion to an enlargement of said magnitude of said external supply voltage.

~~21.~~ 24. (Twice Amended) A semiconductor integrated circuit comprising:

a chip;

a first circuit provided on said chip;

a second circuit provided on said chip;

an internal power supply means, provided on said chip, for supplying an internal supply voltage which is smaller than an external supply voltage;

a reference voltage generating means, provided on said chip, for generating a reference voltage;

wherein said reference voltage provided by said reference voltage generating means is fed to said internal power supply means, said internal supply voltage provided by said internal power supply means is fed to said second

circuit, and said external supply voltage is fed to said first circuit, and a breakdown voltage of a first transistor having thereto said external supply voltage is higher than a breakdown voltage of a second transistor having fed thereto said internal supply voltage, [and] wherein, when the magnitude of said external supply voltage is not larger than that of a predetermined first voltage, the internal supply voltage of said internal power supply means changes at a first rate, when said external supply voltage is between a level exceeding said first voltage and a predetermined second voltage, said internal supply voltage changes at a second rate which is smaller than said first rate, and after said external supply voltage exceeds said second voltage, said internal supply voltage changes at a third rate which is larger than the second rate, wherein the magnitude of said internal supply voltage changing at said second rate is not smaller but larger than that of said internal supply voltage changing at said first rate, [and] wherein said internal supply voltage changing at said third rate enables testing of said second circuit, and wherein the magnitude of said internal supply voltage becomes larger without decreasing in proportion to an enlargement of said magnitude of said external supply voltage.

36

~~22~~. (Twice Amended) A semiconductor integrated circuit comprising:

a substrate;

a first circuit, provided on said substrate, having a first transistor; a second circuit, provided on said substrate, having a second transistor;

an internal power supply [mans] means, provided on said substrate, for supplying an internal supply voltage which is smaller than an external supply voltage;

a reference voltage generating means, provided on said substrate, for generating a reference voltage;

wherein said internal supply voltage provided by said internal power supply means is fed to said second circuit, said external supply voltage is fed to said first circuit and said internal power supply [mean] means includes a converter transistor which outputs said internal supply voltage, said converter transistor having a control electrode; and

wherein said internal supply voltage is controlled by said reference voltage supplied to said control electrode of said converter transistor, [and] wherein, when the magnitude of said external supply voltage is not larger than that of a predetermined first voltage, the internal supply voltage of said internal power supply means changes at a first rate, when said external supply voltage is between a level exceeding said first voltage and a predetermined second voltage, said internal supply voltage changes at a second rate which is smaller than said first rate, and after said external supply voltage exceeds said second voltage, said internal supply voltage changes at a third rate which

is larger than the second rate, wherein the magnitude of said internal supply voltage changing at said second rate is not smaller but larger than that of said internal supply voltage changing at said first rate, [and] wherein said internal supply voltage changing at said third rate enables testing of said second circuit, and wherein the magnitude of said internal supply voltage becomes larger without decreasing in proportion to an enlargement of said magnitude of said external supply voltage.

~~23.~~ 48 (Twice Amended) A semiconductor integrated circuit comprising:

a chip;

an external supply voltage terminal, provided on said chip, for receiving an external supply voltage;

an interface circuit provided on said chip;

an internal circuit provided on said chip;

an internal power supply means, provided on said chip, for supplying an internal supply voltage which is smaller than [an] said external supply voltage;

a reference voltage generating means, provided on said chip, for generating a reference voltage;

wherein said reference voltage provided by said reference voltage generating means is fed to said internal power supply means, [and] wherein, when the magnitude of said external supply voltage is not larger than that of a predetermined first voltage, the internal supply voltage of

said internal power supply means changes at a first rate, when said external supply voltage is between a level exceeding said first voltage and a predetermined second voltage, said internal supply voltage changes at a second rate which is smaller than said first rate, and after said external supply voltage exceeds said second voltage, said internal supply voltage changes at a third rate which is larger than the second rate, wherein the magnitude of said internal supply voltage changing at said second rate is <u>not smaller but</u> larger than that of said internal supply voltage changing at said first rate, [and] wherein said internal supply voltage changing at said third rate enables testing of said [second] <u>internal</u> circuit <u>and wherein the magnitude of said internal supply voltage becomes larger without decreasing in proportion to an enlargement of said magnitude of said external supply voltage</u>.

~~24~~ 61. (Twice Amended) A semiconductor integrated circuit comprising:

a chip;

a load circuit provided on said chip;

internal power supply means provided on said chip for changing an external supply voltage to an internal supply voltage smaller than said external supply voltage within said chip and supplying it to said load circuit;

a reference voltage generation means, provided on said chip, for generating a reference voltage;

wherein said load circuit is fed said internal supply voltage, said internal supply means [is applied by] <u>receives</u> a control signal when said load circuit [flows] <u>carries</u> a relative large current and wherein a driving ability of said internal supply [mean sis] <u>means is</u> increased in response to said control signal.

Claim 27, line 3, delete "first" and insert --third--.

Claim 28, line 2, delete "first" and insert --third--.

Claim 29, line 3, delete "first" and insert --third--.

Claim 30, line 2, delete "first" and insert --third--.

Claim 32, line 2, delete "first" and insert --third--.

Claim 33, line 2, delete "first" and insert --third--.

Claim 61, line 2, delete "first" (first occurrence) and insert --third--.

Claim 62, line 2, delete "first" (first occurrence) and insert --third--.

REMARKS

Claim 1, as identified in the April 16, 1992 Amendment was objected to by the Examiner being that it should have been indicated as claim 7. Applicants acknowledge the Examiner's renumbering of the claim 1 of the April 16, 1992 Amendment as claim 7. This renumbering is reflected in the present Amendment.

Claims 13, 15, 17-20, 22, 24-33, 43-51, 61, 62, 65, 66 and 69 stand rejected under 35 USC 112, second paragraph as